REMARKS

The above-identified patent application has been amended and reconsideration and re-examination are hereby requested.

Claim 18 has been cancelled.

The rejection on grounds of double patenting is a provisional rejection and will be addressed upon the allowance of claims in this patent application or the related application.

Claim 1 has been amended to correct a minor typographical, grammatical error.

The Examiner has rejected Claims 1-17 under 35 USC 103 as being unpatentable Stolt et al., in view of Gates et al.

The Examiner takes the position in paragraph 7 that a data rebuffering section in Stolt et al. is adapted to couple data from one of a plurality of data ports to a data port of a microprocessor selectively in accordance with a control signal. The Examiner brought to the Applicant's attention in paragraph 9, however, "that data ***may not be directly*** passed from the DC to the data ports of the microprocessors but that data port DC in fig. 2 is still a data port." (Emphasis added) Claim 1 specifically states that "(i) a data rebuffering section adapted ***to couple data*** from one of a plurality of data ports to a data port of the microprocessor selectively in accordance with a control signal". Thus, the rejection is not understood because the Examiner admits that Stolt et al shows a system where data " ***may not be directly*** passed from the DC to the data ports of the microprocessors " yet this feature is a specific limitation in the claims.

In view of the fact that, for reason set forth above, the Examiner appears, as understood, to be taking an inconsistent position, Applicant suggests that the Examiner call the Applicant's attorney in order to clarify the apparent inconsistent position of the Examiner and thereby avoid an unnecessary appeal.

In the event any additional fee is required, please charge such amount to Patent and Trademark Office Deposit Account No. 50-0845.

Respectfully submitted,

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Date

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Attachment: Claim Mark Up Sheets
emc-032pus-response to office action dated 031202

VERSION OF CLAIMS WITH MARKINGS TO SHOW CHANGES MADE

1. (Twice Amended) A microprocessor interface disposed between a main memory and a microprocessor, such interface comprising:

a semiconductor integrated circuit having formed therein:

(i) a data rebuffering section adapted to couple data from ~~a~~ one of a plurality of data ports to a data port of the microprocessor selectively in accordance with a control signal; and

(ii) a main memory interface adapted for coupling to the main memory for the microprocessor, such main memory interface being coupled to the data rebuffering section for providing control signals to the main memory for enabling data transfer between the main memory and the microprocessor through the data rebuffering section.

2. The microprocessor interface recited in claim 1 wherein the main memory is a selected one of a plurality of memory types each type having a different data transfer protocol and wherein the main memory interface is configured in accordance with the selected one of the plurality of memory types to provide a proper memory protocol to data being transferred between the microprocessor and the main memory through the main memory interface.

3. The microprocessor interface recited in claim 2 wherein one main memory type is an SDRAM.

4. The microprocessor interface recited in claim 2 wherein one main memory type is a RDRAM.

5. The microprocessor interface recited in claim 1 including a second integrated circuit adapted for controlling the first- mention integrated circuit, such second integrated circuit having

9. The microprocessor interface recited in claim 8 wherein the main memory is a selected one of a plurality of memory types each type having a different data transfer protocol and wherein the main memory interface is configured in accordance with the selected one of the plurality of memory types to provide a proper memory protocol to data being transferred between the microprocessor and the main memory through the main memory interface.

10. The microprocessor interface recited in claim 9 wherein one main memory type is an SDRAM.

11. The microprocessor interface recited in claim 9 wherein one main memory type is a RDRAM.

12. The microprocessor interface recited in claim 9 wherein the main memory interface comprises:

a microprocessor/main memory interface control section adapted to provide control signals between such section and the microprocessor and between such section and the controller; and

a main memory controller, such controller being configured in accordance with the selected one of the plurality of memory types to provide the proper memory protocol to data being transferred between the microprocessor and the main memory through the main memory interface.

13. The microprocessor interface recited in claim 9 wherein the main memory interface comprises:

a microprocessor/main memory interface control section adapted to provide control signals between such section and the microprocessor and between such section and the

controller; and

a main memory controller, such controller being configured in accordance with a control signal provided thereto by the microprocessor to address a selected one of the plurality of potential memory capacities, the control signal supplied by the microprocessor indicating to the main memory controller the particular one of the plurality of potential memory capacities of the main memory.

14. The microprocessor interface recited in claim 13 wherein the main memory interface comprises:

a microprocessor/main memory interface control section adapted to provide control signals between such section and the microprocessor and between such section and the controller; and

a main memory controller, such controller being configured in accordance with the selected one of the plurality of memory types to provide a proper memory protocol to data being transferred between the microprocessor and the main memory through the main memory interface.

15. The microprocessor interface recited in claim 14 wherein one main memory type is an SDRAM.

16. The microprocessor interface recited in claim 14 wherein one main memory type is a RDRAM.

17. The microprocessor interface recited in claim 14 wherein the main memory interface includes an error correction and detection unit coupled between the distributor and the main memory controller.

~~18. The microprocessor interface recited in claim 17 wherein the microprocessor is a Power PC microprocessor.~~

19. The microprocessor interface recited in claim 5 including a mask to transform the address to an address in the second section of the memory.